CLAIMS

WHAT IS CLAIMED IS:

1. An apparatus for testing an integrated circuit chip, comprising:

a printed circuit device having connector pads, contacts, and traces extending between at least some of the connector pads and the contacts, wherein the printed circuit device has openings therethrough, intersecting the contacts, that are adapted to receive pins extending from the integrated circuit chip so that the contacts may electrically contact the pins extending from the integrated circuit chip; and

a connector electrically interconnected with at least some of the connector pads,

wherein the apparatus is adapted to be disposed between the integrated circuit chip and a chip socket, such that the pins extending from the integrated circuit chip may be inserted through the printed circuit device and into the chip socket.

2. An apparatus, according to claim 1, wherein the printed circuit device further comprises:

a first flexible dielectric layer having a first surface and a second surface;

a second flexible dielectric layer having a first surface; and

an adhesive layer bonding the first surface of the first flexible layer and the first surface of the second flexible layer,

wherein the contacts and the traces are disposed on the first surface of the first flexible dielectric layer, the connector pads extend through the first flexible dielectric layer to the first surface of the first flexible dielectric layer and the second surface of the first flexible dielectric layer, and the second flexible dielectric layer substantially covers the first surface of the first flexible dielectric layer, the connector pads, the contacts, and the traces.

3. An apparatus, according to claim 2, wherein the first flexible dielectric layer and the second flexible dielectric layer are made of a polyimide material.

4. An apparatus, according to claim 2, wherein the adhesive layer is comprised of a material selected from the group consisting of an acrylic adhesive or an epoxy adhesive.

5. An apparatus, according to claim 1, wherein the printed circuit device has a thickness no greater than about 0.5 mm.

6. An apparatus, according to claim 1, wherein the printed circuit device has a lower surface and wherein the apparatus further comprises a backing plate attached to the lower surface of the printed circuit device.

7. An apparatus, according to claim 6, further comprising a fastener for attaching the backing plate to the lower surface of the printed circuit device.

8. An apparatus, according to claim 6, wherein the backing plate is made of a dielectric material.

9. An apparatus, according to claim 1, wherein the printed circuit device further comprises a plurality of layers of contacts and traces.

10. An apparatus, according to claim 9, wherein the plurality of layers of contacts and traces further comprises a plurality of flexible dielectric layers on which the layers of contacts and traces are disposed and wherein the plurality of flexible dielectric layers are adhesively bonded to one another.

11. A test assembly, comprising:

an integrated circuit chip having pins extending therefrom;

a chip socket having contacts engaged with the pins extending from the integrated circuit chip;

a printed circuit device disposed between the integrated circuit chip and the chip socket; and

a connector,

wherein the printed circuit device has connector pads, contacts, and traces extending between the contacts and at least some of the connector pads;

wherein the printed circuit device has openings therethrough, intersecting the contacts, through which the pins extending from the integrated circuit chip are disposed such that the contacts are engaged with the pins extending from the integrated circuit chip; and

wherein the connector is electrically connected with at least some of the connector pads.

12. A test assembly, according to claim 11, further comprising a motherboard electrically interconnected with the chip socket.

13. A test assembly, according to claim 11, further comprising a daughtercard electrically interconnected with the chip socket.

14. A test assembly, according to claim 11, wherein the printed circuit device further comprises:

a first flexible dielectric layer having a first surface and a second surface;

a second flexible dielectric layer having a first surface; and

an adhesive layer bonding the first surface of the first flexible dielectric layer and the first surface of the second flexible dielectric layer,

wherein the contacts and the traces are disposed on the first surface of the first flexible dielectric layer, the connector pads extend through the first flexible dielectric layer to the first surface of the first flexible dielectric layer and the second surface of the first flexible dielectric layer, and the second flexible dielectric layer substantially covers the first surface of the first flexible dielectric layer, the connector pads, the contacts, and the traces.

15. A test assembly, according to claim 14, wherein the first flexible dielectric layer and the second flexible dielectric layer are made of a polyimide material.

16. A test assembly, according to claim 14, wherein the adhesive layer is comprised of a material selected from the group consisting of an acrylic adhesive or an epoxy adhesive.

17. A test assembly, according to claim 11, wherein the printed circuit device has a thickness no greater than about 0.5 mm.

18. A test assembly, according to claim 11, wherein the printed circuit device has a lower surface and wherein the test assembly further comprises a backing plate attached to the lower surface of the printed circuit device.

19. A test assembly, according to claim 18, further comprising a fastener for attaching the backing plate to the lower surface of the printed circuit device.

20. A test assembly, according to claim 18, wherein the backing plate is made of a dielectric material.

21. A test assembly, according to claim 11, wherein the printed circuit device further comprises a plurality of layers of contacts and traces.

22. A test assembly, according to claim 21, wherein the plurality of layers of contacts and traces further comprises a plurality of flexible dielectric layers on which the layers of contacts and traces are disposed and wherein the plurality of flexible dielectric layers are adhesively bonded to one another.

23. A test assembly, according to claim 11, wherein the contacts of the chip socket and the contacts of the printed circuit device are removably engaged with the pins extending from the integrated circuit chip.

24. A test assembly, according to claim 11, further comprising a testing device, electrically interconnected with the connector, for testing the integrated circuit chip.

25. A method, comprising inserting a test adapter between an integrated circuit chip and a chip socket such that pins extending from the integrated circuit chip are physically connected with contacts of the test adapter and with contacts of the chip socket.

26. A method, according to claim 25, further comprising attaching a testing device to the test adapter to test a function of the integrated circuit chip.

27. A method, according to claim 25, further comprising inputting a signal to the integrated circuit chip via the test adapter.

28. A method, according to claim 25, further comprising monitoring a signal outputted from the integrated circuit chip via the test adapter.

29. A method, according to claim 25, further comprising testing the integrated circuit chip via the test adapter while the integrated circuit chip is in operation in a computer system.

30. An apparatus, comprising means for inserting a test adapter between an integrated circuit chip and a chip socket such that pins extending from the integrated circuit chip are physically connected with contacts of the test adapter and with contacts of the chip socket.

31. An apparatus, according to claim 30, further comprising means for attaching a testing device to the test adapter to test a function of the integrated circuit chip.

32. An apparatus, according to claim 30, further comprising means for inputting a signal to the integrated circuit chip via the test adapter.

33. An apparatus, according to claim 30, further comprising means for monitoring a signal outputted from the integrated circuit chip via the test adapter.

34. An apparatus, according to claim 30, further comprising means for testing the integrated circuit chip via the test adapter while the integrated circuit chip is in operation in a computer system.